

# Performance Analysis of Digital Flux-locked Loop Circuit with Different SQUID $V$ - $\phi$ Transfer Curves for TES Readout System\*

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A superconducting quantum interference device (SQUID), functioning as a nonlinear response device, typically requires the incorporation of a flux-locked loop (FLL) circuit to facilitate linear amplification of the current signal transmitted through a superconducting transition-edge sensor (TES) across a large dynamic range. This work presents a reasonable model of the SQUID-FLL readout system, based on a digital proportional-integral-differential (PID) flux negative feedback algorithm. This work investigates the effect of  $V$ - $\phi$  shape on the performance of digital FLL circuits. Such as the impact factors of bandwidth, design limits of slew rate of the system and the influence of the shapes of SQUID  $V$ - $\phi$  curve. Furthermore, the dynamic response of the system to X-ray pulse signals with rise time ranging from 4.4~281  $\mu$ s and amplitudes ranging from 6~8  $\phi_0$  was simulated. All the simulation results were found to be consistent with the existing mature theories, thereby validating the accuracy of the model. The results also provide a reliable modelling reference for the design of digital PID flux negative feedback and multiplexing SQUID readout electronic systems.

Keywords: TES, SQUID, Digital flux-locked loop, Readout system.

## I. INTRODUCTION

As an ultra low-noise detector, a superconducting transition-edge sensor (TES) can achieve an energy resolution ranging from several to several tens of eV [1–3]. To ensure a high signal-to-noise ratio of TES, a low-noise direct current superconducting quantum interference device (SQUID) is typically used to couple the TES current and then readout [4]. However, SQUID is a nonlinear device that can only guarantee linear amplification of the signal over a very small dynamic range. To enable the nonlinear SQUID to amplify the TES signal linearly over a larger dynamic range, it is necessary to construct a flux negative feedback lock loop (FLL) [5].

A significant benefit of employing a digital system to control a SQUID is the convenient manipulation of digitized signals. For example, the analog integrator and its reset circuit can be easily set up using just a few lines of code [6, 7]. The reset circuit not only automatically resets the position of the  $V$ - $\phi$  curve prior to the SQUID lock, but also automatically adjusts the position of the FLL circuit working (locking) point. It has been demonstrated that digital FLL has the capacity to increase the dynamic input range of a SQUID to a substantial degree by using flux-quanta counting and dynamic field compensation (DFC) methods [8]. The noise spectral

density measurement shows that the digital FLL system performs in a similar way to the analog FLL controller in previous work [9]. The digital FLL is now widely used in experiments such as magnetoencephalogram (MEG) [10], magnetocardiogram (MCG) [11], cosmic microwave background (CMB) [12], X-ray and  $\gamma$ -ray detection [13, 14]. Previous works mainly focus on digital FLL noise in these experiments and lack a detailed description of the parameters that affect digital FLL system performance. For example, it is necessary to have fast response in X-ray detection, which requires the FLL to have a large slew rate, typically several  $\mu$ s at 10  $\mu$ A [15], which is less than 2  $\phi_0$  if the mutual inductance coefficient of SQUID coil is 5  $\mu$ A/ $\phi_0$ . In CMB detection experiments, the design of digital FLL requires large bandwidth in order to improve multiplexing numbers of readout channels [16]. In order to understand the performance of the digital SQUID-FLL system and to design higher performance readout circuits, we simulate the functional upper limits of SQUID-FLL system. Little previous works has investigated the effect of different shapes of SQUID  $V$ - $\phi$  curves on the performance of digital FLL systems. Therefore we analyze the effect of shapes on the performance of digital FLL using three different shapes of SQUID  $V$ - $\phi$  curve models.

The paper is organized as follows: In Section II, a sinusoidal-like approximation is made to the SQUID flux response model, and the fundamentals of the digital SQUID-FLL circuit are introduced. In Section III, we conduct a comprehensive simulation analysis to validate the reliability of the model. This primarily entails simulations of the fundamental linear amplification readout function of the input magnetic flux signal, system bandwidth, and slew rate. Finally, the dynamic response of the system was simulated using pulse signals that were designed to resemble actual TES pulse signals with varying rise time and amplitudes. This SQUID-FLL

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readout system model can provide reliable design references for digital flux negative feedback (DFB) readout and multiplexing SQUID readout systems. Section IV concludes the paper.

## II. PRINCIPLE OF DIGITAL SQUID-FLL MODEL

### A. Simplified SQUID transfer model

The circuit model of the SQUID-FLL is illustrated in Figure 1. It is comprised of a single-stage SQUID. The current signal flowing through the TES is coupled with the input coil  $L_{in}$  and converted into a magnetic flux signal  $\phi_{in}$ . Although different designs for the SQUIDs exhibit varying responses to input magnetic flux  $\phi_{in}$ , and all have common character-

istics: the response of SQUID to  $\phi_{in}$  is periodic and nonlinear, which resembles a quasi-sinusoidal curve [17]. Following magnetic flux locking, the error between the input and feedback magnetic flux is nearly zero, maintaining the total flux value in the SQUID at the working point. Theoretically, we only need to know the linear conversion coefficient of  $dV_{SQUID}/d\phi_{in}$  at the lock point [18] but do not need to care any shape of the  $V$ - $\phi$  response curve of SQUID, where  $V_{SQUID}$  represents the voltage across SQUID. To prove this point, we simulate the FLL circuit for different SQUID flux response cases in Section III.

We simplify the SQUID  $V$ - $\phi$  transfer model to a standard sinusoidal function. Assuming that the mutual inductance coefficient of the SQUID input coil is  $M_{in}$  and the mutual inductance coefficient of the feedback coil is  $M_{fb}$ , the relationship between the error signal  $u_{err}(t)$  and the input and feedback magnetic fluxes can be expressed as follows:

$$u_{err}(t) = A \sin \left( \frac{2\pi}{\phi_0} \left[ i_{in}(t)M_{in} - \frac{u_o(t)M_{fb}}{R_{fb}} + \phi_{offset} \right] \right) G_1 + u_{offset} \quad (1)$$

where  $\phi_0$  denotes the quantum magnetic flux.  $i_{in}(t)$  is the TES signal through the input coil and the input flux is given by  $\phi_{in} = i_{in}(t)M_{in}$ .  $\phi_{offset}$  is the magnetic flux bias applied to the input or feedback coils.  $u_o(t)$  denotes the feedback voltage signal.  $R_{fb}$  denotes the feedback resistor and the feedback magnetic flux is given by  $\phi_{fb} = \frac{u_o(t)M_{fb}}{R_{fb}}$ .  $G_1$  denotes the linear gain of the room low-noise preamplifier.  $A$  denotes the amplitude of the voltage across the SQUID.  $u_{offset}$  denotes the voltage offset of the amplifier.

### B. Principle of digital FLL

The fundamental structure of the FLL is the construction of a closed-loop negative flux feedback circuit based on operational amplifiers [19], as shown in the left part of Figure 1. By analyzing the current relationships contained within the green dashed line in Figure 1, we can derive the circuit equation relating the output digital signal  $u_o(n)$  to the input error signal  $u_{err}(n)$ :

$$u_o(n) = \left( \frac{R_2}{R_1} + \frac{C_1}{C_2} \right) u_{err}(n) + \frac{\Delta t}{R_1 C_2} \sum_{i=0}^n u_{err}(i) + \frac{R_2 C_1}{\Delta t} [u_{err}(n) - u_{err}(n-1)] \quad (2)$$

where  $R_1$  and  $C_1$  are the input resistance and capacitance, respectively.  $R_2$  and  $C_2$  are the feedback resistance and capacitance, respectively.  $P \equiv \left( \frac{R_2}{R_1} + \frac{C_1}{C_2} \right)$  is a proportional parameter.  $I \equiv \frac{\Delta t}{R_1 C_2}$  is the integral parameter.  $D \equiv \frac{R_2 C_1}{\Delta t}$  is the

differential parameter.  $\Delta t$  represents the digital sampling period.  $u_{err}(i)$  denotes the  $i$ -th sampled error signal after amplification by  $G_1$ .  $u_{err}(n)$  is the average value of all sampled  $u_{err}(i)$  in one frame as shown in Figure 2.  $u_o(n)$  is the  $n$ -th output (feedback) signal. Similarly, by digitizing Equation 1, we obtain:

$$u_{err}(i) = A \sin \left( \frac{2\pi}{\phi_0} \left[ i_{in}(i)M_{in} - \frac{u_o(n)M_{fb}}{R_{fb}} + \phi_{offset} \right] \right) G_1 + u_{offset} \quad (3)$$

The primary objective of the PID algorithm design is to calibration of the three aforementioned parameters. If these

parameters are not adequately calibrated, system oscillations can occur, which may lead to an extended time to lock (track)

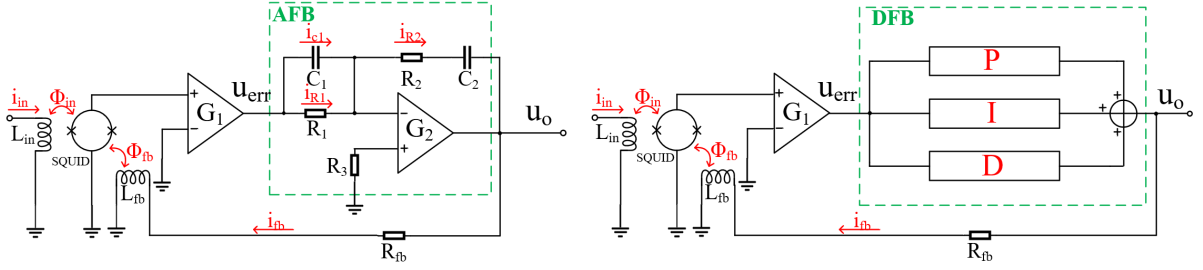


Fig. 1. SQUID-FLL readout circuit model.  $\phi_{in}$  is the input flux signal and  $\phi_{fb}$  is the feedback flux.  $G_1$  is linear gain of room temperature preamplifier. The left figure shows the principle design of analog SQUID-FLL circuit. The right figure is the equivalent digital PID circuit. Analog feedback (AFB) and digital feedback (DFB) circuits are included in the green dashed lines.

the signal or even a loss of lock.

### III. DIGITAL SQUID-FLL PERFORMANCE ANALYSIS

#### A. Basic characterization of digital SQUID-FLL system

In our simulation, we emulated the typical conditions employed in laboratory tests, assuming that the SQUID is biased at a position with a substantial voltage swing prior to flux locking. The current through TES  $i_{in}(i)$  serves as the input reference for the SQUID input coil  $L_{in}$ . The default parameters used in the simulation, unless otherwise specified, are listed in Table 1.

Table 1. Default simulation parameters of SQUID-FLL system.

Parameter	Value
Input signal type	Triangle Wave
Input signal frequency	23 Hz
Input signal amplitude	50 $\mu$ A
Testing time	50 ms
Digital sample rate	150 MSPS
Sample numbers per feedback	7
Mutual inductance of input coil $1/M_{in}$	28 $\mu$ A/ $\phi_0$
Mutual inductance of feedback coil $1/M_{fb}$	38 $\mu$ A/ $\phi_0$
Conversion coefficient $dV_{SQUID}/d\phi_{in}$ at lock point	3 mV/ $\phi_0$
Input resistor $R_1$	100 $\Omega$
Feedback resistor $R_2$	50 $\Omega$
Input capacitor $C_1$	0 nF
Feedback capacitor $C_2$	1 nF
Feedback resistor $R_{fb}$	10 k $\Omega$
Preamplifier gain $G_1$	100
Voltage amplitude across SQUID Array	700 $\mu$ V
Preamplifier voltage offset $u_{offset}$	0 $\mu$ V
Flux offset $\phi_{offset}$	0 $\mu\phi_0$
Settle time $t_{set}$	0 ns

The rise time of TES's signals are typically from several  $\mu$ s to several tens of ms [20, 21]. Consequently, the feedback algorithm design does not require consideration of future trend predictions. Consequently, in the default settings, the input capacitance  $C_1$  was set to 0, retaining only the P and I components. Considering the prospective system design, the digital sampling time was established at 150 MSPS, with seven

points sampled in each frame. The frame clock (feedback frequency) was approximately 21.4 MHz, and the effective system Nyquist bandwidth is approximately 10.7 MHz. In digital feedback, the error signal from the current frame is used to compute the feedback signal for the next frame, which results in a delayed feedback loop. This process is analogous to time-division multiplexing (TDM) SQUID readout logic, with the exception of row selection [22, 23]. In this configuration, the frame frequency is equal to the row selection frequency in the TDM. The timing logic is illustrated in Figure 2. Average value of the error signal,  $u_{err}(n)$ , is calculated from the  $u_{err}(i)$  to  $u_{err}(i+6)$  values in the  $n$ -th frame. The feedback signal  $u_o(n)$  is then calculated for the next frame. It should be noted that our model does not take into account other system delays, which typically amount to several hundred nanoseconds and may include transmission line delays. While these delays may reduce the system bandwidth, they do not impact the model's behaviour. Prior to the locking of the SQUID, it is essential to adjust the locking work point. Typically, in order to ensure linear amplification with no offset, the lock point is selected at the zero point of the input flux ( $\phi_{in} = 0$ ) and the zero point of the output (feedback) flux ( $\phi_{fb} = 0$ ). The initial error signal is set to 0. The bias signals  $\phi_{offset}$ ,  $u_{offset}$  and settle time  $t_{set}$  are also set to 0. The results of the feedback locking are shown in Figure 3. The absolute error signal does not exceed 10  $\mu\phi_0$ , and the calculated relative error signal is less than 0.1 %.

The locking conditions were simulated under different flux and voltage offset conditions. In typical circumstances, the response of the input flux  $dV_{SQUID}/d\phi_{in}$ , near the SQUID locking point, must have the opposite polarity as the room temperature amplifier gain to ensure that the SQUID locking point is maintained. This is shown in Figures 4 (a) and (c). In the event that the polarity of the room temperature amplifier gain is identical to that of the SQUID response, a locking point offset phenomenon is observed, as illustrated in Figure 4 (b). In order to verify the independence of the FLL circuit from the shape of the SQUID  $V$ - $\phi$  response curve, as illustrated in Section II A, we simulate flux locking for different shapes of the SQUID  $V$ - $\phi$  curve, as shown in Figure 5.

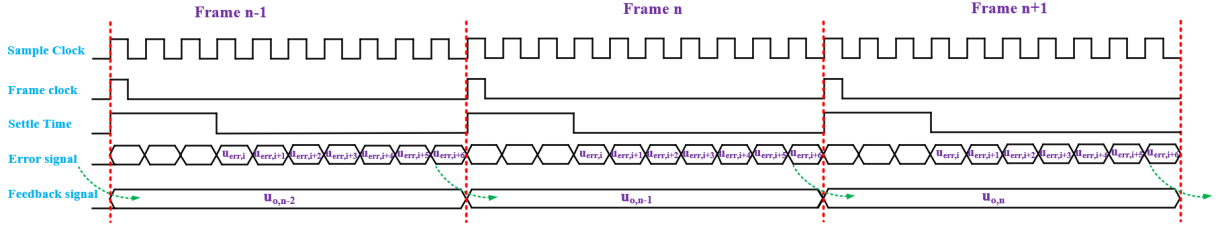


Fig. 2. Time logic of digital sample frequency and frame clock (feedback frequency). Sampled error signals are used to calculate next frame feedback signal based on PID algorithm.

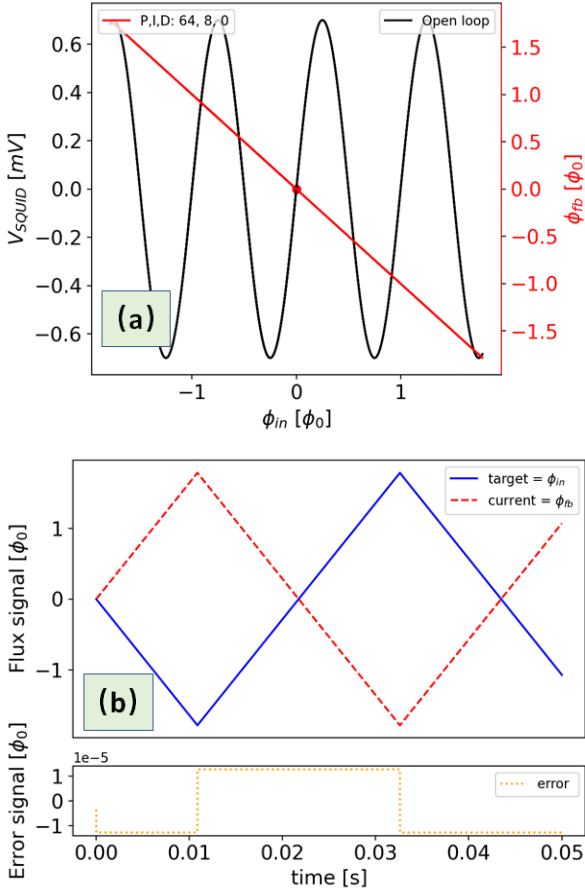


Fig. 3. Simulation result of SQUID-FLL model based on PID algorithm with low frequency triangle wave. (a) Black line show the relationship between output flux  $\phi_{fb}$  and input flux  $\phi_{in}$  without flux lock loop. Red line shows the locked linear gain with default PID parameters at lock point (red dot). All PID parameters on the legend are relative values calculated according to Table 1 and shifted 7 bits to the left. (b)  $\phi_{fb}$  (red dashed line) tracks  $\phi_{in}$  (blue solid line) in time domain after flux lock. The orange dotted line below shows the tracked flux error, which is less than  $10 \mu\phi_0$ .

### B. Bandwidth and slew rate of digital SQUID-FLL system

When designing a SQUID-FLL circuit, it is essential to consider the rational design of the system bandwidth, par-

ticularly in multiplexing experiments. An FLL with a small bandwidth may result in distortion of the TES signal, whereas a larger bandwidth could introduce additional high-frequency noise, which would in turn affect the energy resolution of the TES. The effect of different feedback capacitors  $C_2$  (integral component) and different shapes of  $V$ - $\phi$  transfer curves on the bandwidth was simulated, and the results are shown in Figure 6. In Figure 6, we consider the ideal case, without considering digital circuit delays ( $t_{set} = 0$ ), as in analog FLL. All SQUID  $V$ - $\phi$  curves have same conversion coefficient  $dV_{SQUID}/d\phi_{in}$  at the locking point and linear dynamic input range. The PID feedback is a time-domain simulation. By comparing it with the frequency-domain transfer function of the system, the correctness of the SQUID-FLL models can be verified. Based on frequency-domain transfer function [17], the theoretical 3 dB system bandwidth can be obtained:

$$f_c \approx \frac{V_\phi G_1 M_{fb}}{2\pi R_1 C_2 R_{fb}} \quad (4)$$

where  $V_\phi = dV_{SQUID}/d\phi_{in}$  denotes the conversion coefficient at the locking point. For example, when  $C_2 = 2$  nF, the calculated value for the critical frequency  $f_c$  based on Equation 4 is 628 kHz, which is in accordance with the results of different  $V$ - $\phi$  transfer models displayed in Figure 6. From Equation 4, it can be observed that a multitude of factors influence bandwidth, all of which are linearly correlated. In room temperature circuit design, the bandwidth can be determined by adjusting the preamp gain  $G_1$ , input resistance  $R_1$ , feedback capacitance  $C_2$ , and feedback resistance  $R_{fb}$ . It is crucial to acknowledge that  $G_1$  represents an ideal linear gain in the simulation. In an actual design, the limitations of the operational amplifier's gain bandwidth product (GBP) must be considered. Therefore, this gain should not be excessively large for a system with a large bandwidth. Furthermore, in a practical design, system delays also reduce the bandwidth, necessitating the minimization of cable lengths. If the system delay is considered ( $t_{set} \neq 0$ ), the system bandwidth should satisfy Equation 5 and the simulation results are shown in Figure 7.  $t_{sp}$  is the ADC sampling period and  $N_{sp}$  is the number of samples.  $t_{fm}$  is the frame period.

$$f_c \approx \frac{V_\phi G_1 M_{fb} N_{sp} t_{sp}}{2\pi R_1 C_2 R_{fb} t_{fm}} \quad (5)$$

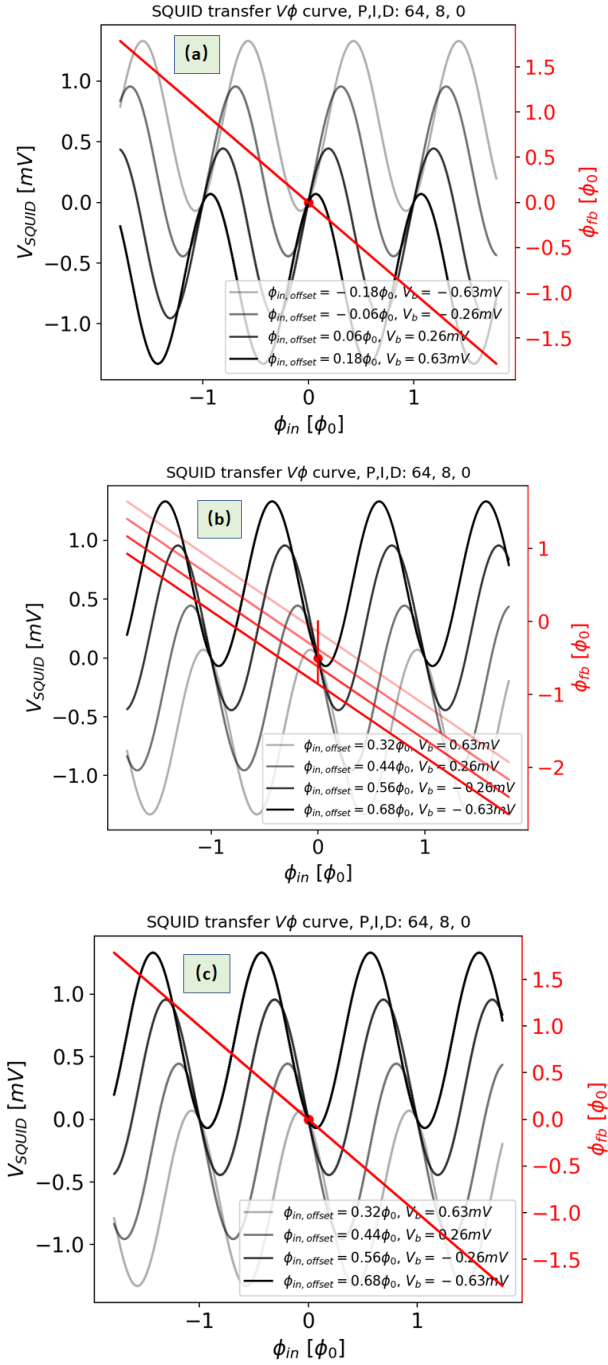


Fig. 4. Simulation results of SQUID-FLL model (red lines) under different flux offsets  $\phi_{in, offset}$  and voltage offsets  $V_b$  (black lines).  $V_b$  is added after  $G_1$  (a) Results at different flux offset when room amplification gain is negative and  $dV_{SQUID}/d\phi_{in} > 0$  at locking point. (b) Room amplification gain is negative but  $dV_{SQUID}/d\phi_{in} < 0$  at locking point. Locking point offset appears. (c) Room amplification gain is positive and  $dV_{SQUID}/d\phi_{in} < 0$  at locking point.

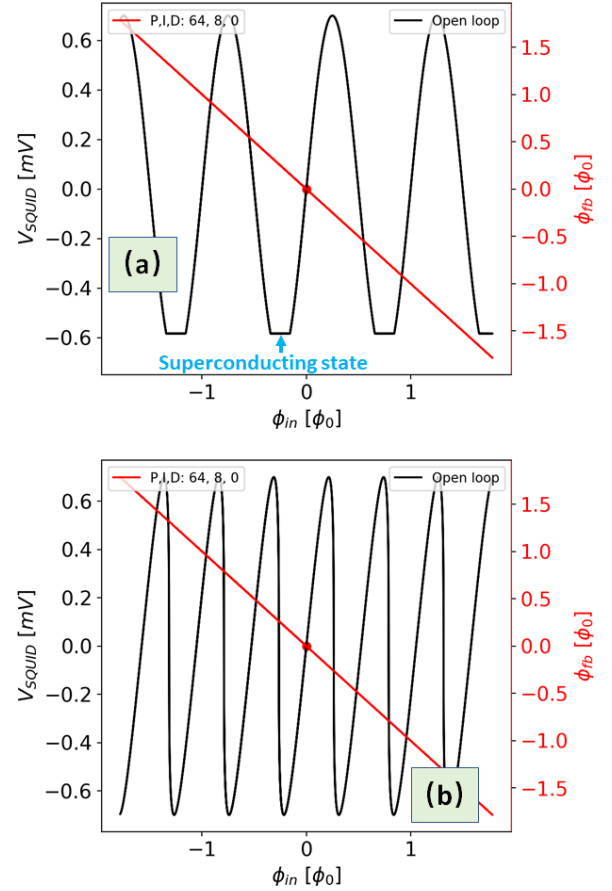


Fig. 5. Simulation results of SQUID-FLL (red lines) under varying SQUID  $V\phi$  response. (a) SQUID lock status at small bias current. The superconducting state exists at this moment. (b) Lock status at asymmetric response.

Further investigation was conducted on the system slew rate  $\partial\phi_{fb}/\partial t$ . When the bandwidth is sufficiently large but the slew rate is too small, it can also lead to signal distortion. The system slew rate is determined jointly by the bandwidth, the input range  $\phi_{lin}$  of the SQUID's open-loop linear gain, and the design of the FLL integral parameter, and is independent of frequency [18]. This relationship can be expressed as follows:

$$\frac{\partial\phi_{fb}}{\partial t} = \frac{\phi_{lin}N_{sp}t_{sp}}{2R_1C_2t_{fm}} \quad (6)$$

In our SQUID transmission model,  $\phi_{lin} \approx 0.3\phi_0$ , as shown on the top of Figure 6. Based on Equation 6, we calculated  $\partial\phi_{fb}/\partial t \approx 1.5\phi_0/\mu s$ . The simulated result ( $t_{set}=0$ ) was approximately  $1.5\phi_0/\mu s$ , as shown in Figure 8. When the signal rise time exceed  $1.6\mu s$ , the FLL is unable to accurately track the signal, resulting in distortion. It can be seen that when the SQUID transfer model is different, the shape of the tracked signal is different when distortion appears. But the value of the slew rate is same. All signals are distorted at rise times less than  $1.6\mu s$ , which is independent of the shape of the SQUID transfer model. For digital FLL, the slew rate



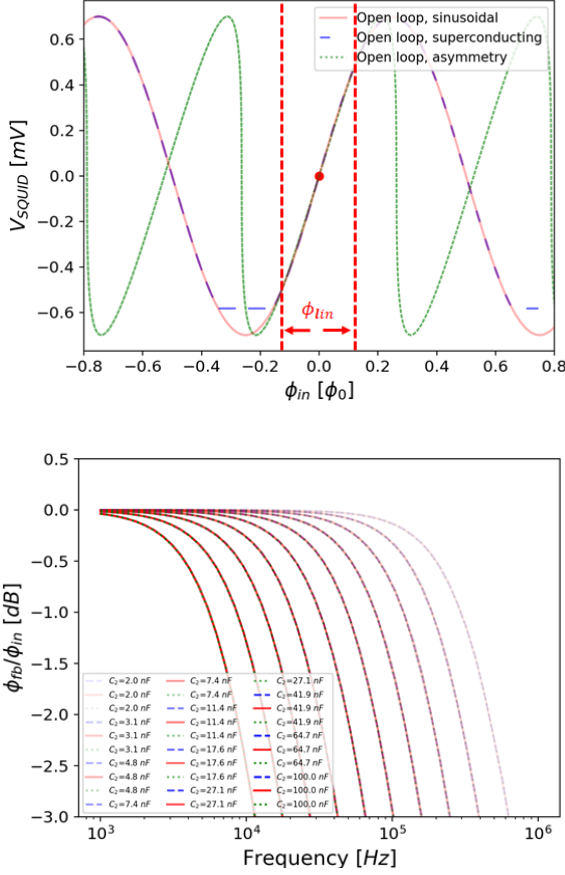


Fig. 6. SQUID-FLL system bandwidth simulation. The top figure shows the same open-loop linear gain input range  $\phi_{lin}$  for three different shapes of  $V-\phi$  response. The red solid line is the sinusoidal-like model. The blue dashed line is the small bias model with superconducting state. The green dotted line is the asymmetrical model. The bottom figure shows the bandwidth with different feedback capacitor  $C_2$  for three varying shapes of  $V-\phi$  curves, which prove that  $V-\phi$  responses of different shapes have equivalent bandwidth when they have same  $V_\phi$  conversion coefficient at the locking point.

decreases when the frame frequency is reduced, as shown in Figure 9. In theory, to track a faster signal, one can adjust the integration parameters, feedback resistance and so forth to modify the bandwidth. According to equations 5 and 6, the ideal linear relationship between slew rate and bandwidth is shown in Figure 10.

### C. Noise contribution in digital FLL system

The TES detector has a high energy resolution mainly due to its small thermal noise at low temperatures. In the experiment, the noise is mainly comprised of TES Johnson noise and thermal fluctuation noise (TFN) [24]. The thermal noise of SQUID and the voltage noise of preamplifier mainly constitute the system's high-frequency noise. For digital FLL circuits, the quantization noise of the ADC and DAC devices

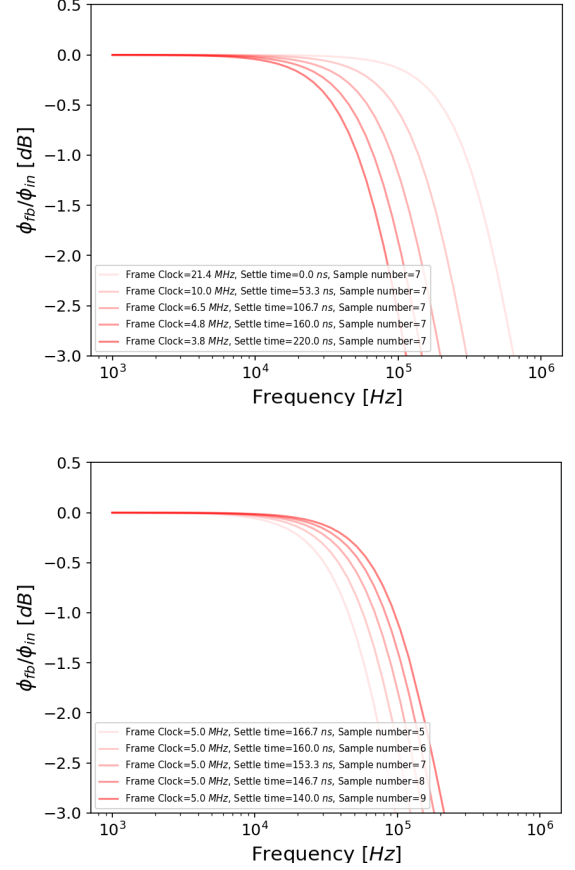


Fig. 7. Simulation results of SQUID-FLL under varying settle time. The top figure shows the bandwidth increases with the frame rate when  $N_{sp}$  is constant. The bottom figure shows the bandwidth increases with  $N_{sp}$  when the frame rate is constant.

also affects the signal-to-noise ratio (SNR). The noise spectral density  $S(f)$  of ADC or DAC should satisfy Equation 7.

$$S(f) = \frac{q}{\sqrt{12}} \frac{1}{\sqrt{BW}} \quad (7)$$

$q$  is the least number bit (LSB) voltage of ADC or DAC.  $BW$  is the Nyquist bandwidth of the system. We can calculate the equivalent current noise density  $S_I(f)$  corresponding to the input coil of SQUID according to Equation 8.

$$S_I(f) = \frac{S(f)}{G_1 V_\phi M_{in}} \quad (8)$$

For example, the equivalent current noise of a 16-bit ADC with 2 V full scale range is  $0.8 \text{ pA}/\sqrt{\text{Hz}}$  refers to the input coil of SQUID, which is far less than the noise of TES (generally several tens to hundreds  $\text{pA}/\sqrt{\text{Hz}}$ ). The equivalent noise of a 16-bit DAC is  $0.6 \text{ pA}/\sqrt{\text{Hz}}$  when the feedback resistor is  $10 \text{ k}\Omega$  as shown in Table 1. Thus, it is better to choose a large feedback resistor and high-resolution ADC and DAC for digital FLL.

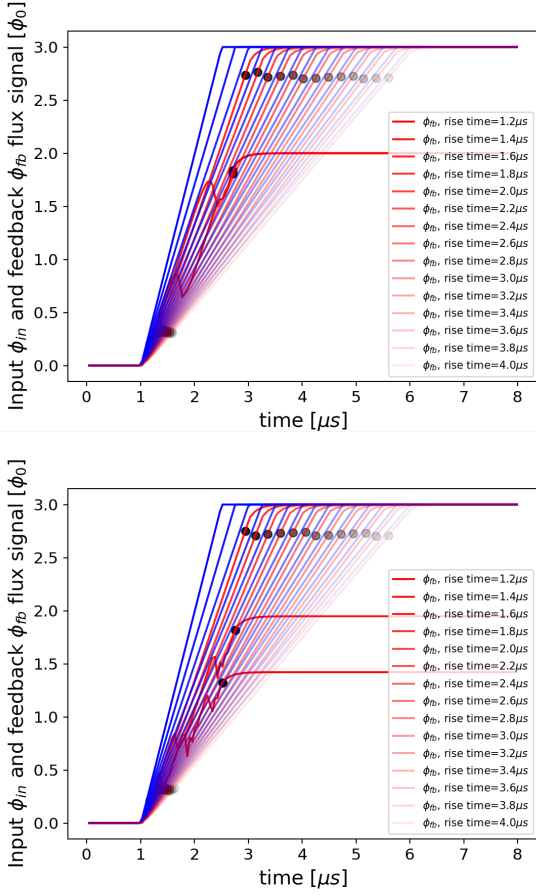


Fig. 8. SQUID-FLL system slew rate simulation. The top figure shows the same maximum slew rate of SQUID-FLL system is about  $1.6 \phi_0/\mu s$  when the SQUID transfer functions are sinusoidal-like model or small bias model with superconducting state. The rise time of  $\phi_{fb}$  (red line) is about  $1.6 \mu s$  and the amplitude of  $\phi_{fb}$  is up to  $3 \phi_0$  without distortion. Rise time is from 10 % to 90% amplitude of signal. The bottom figure shows the same maximum slew rate of SQUID-FLL system based on asymmetrical model.

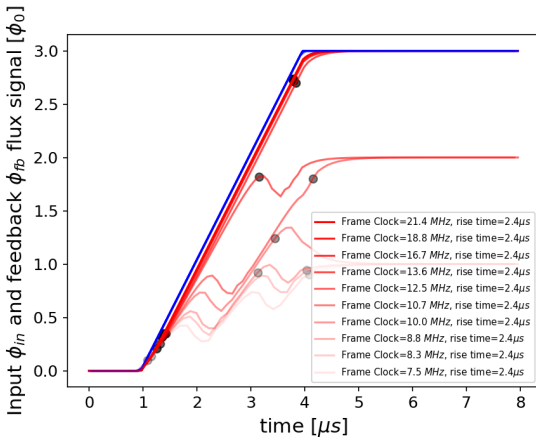


Fig. 9. Tracking  $2.4 \mu s$ ,  $3 \phi_0$  signals at different frame rates. The signal is distorted when the frame rate is reduced to 12.5MHz.

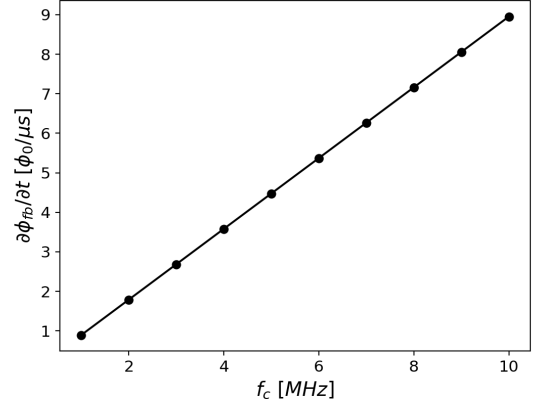


Fig. 10. The ideal relationship between SQUID-FLL system slew rate  $\partial\phi_{fb}/\partial t$  and cutoff frequency  $f_c$ .

#### D. X-ray pulse signal response

Considering that the TES used for X-ray detection has a fast response time of the order of a few microseconds to several hundred microseconds, we used a pulse signal comprising white noise as input to simulate the response process of the X-ray TES. If the Nyquist noise bandwidth is 1 MHz, the noise of the TES system was set to  $50 \text{ pA}/\sqrt{\text{Hz}}$  at 1 kHz and an RMS value of  $22 \mu A$  (refer to the SQUID input coil), which is based on our testing results [25]. We use the sinusoidal-like SQUID-FLL model to demonstrate effective tracking of pulses with varying rise time, as illustrated in Figure 11 (a). Furthermore, a simulation was performed in which the rise time was set at  $4.3 \mu s$  while the pulse amplitude was increased. The results of this simulation are shown in Figure 11 (b). Distortion occurs when the signal amplitude exceeds  $7.8 \phi_0$ . The corresponding slew rate is approximately  $1.45 \phi_0/\mu s$ , which is consistent with the simulation results shown on the right side of Figure 8.

#### IV. CONCLUSION

A comprehensive behavioral simulation of the SQUID-FLL circuit was performed using different SQUID models in conjunction with the principles of digital PID magnetic flux feedback. We demonstrate that the design of the FLL does not depend on the shape of the SQUID  $V-\phi$  response by simulating SQUID transfer function models with three different shapes. A comprehensive list of parameters that must be considered when designing the SQUID-FLL system is presented in Table 1. Common scenarios of locking point adjustments during laboratory tuning were analyzed. The primary factors influencing the design of the system bandwidth  $f_c$  were examined, thereby providing valuable references for the design of SQUIDs and room readout electronics. Finally, the upper limit of the slew rate of the system was thoroughly analyzed, and it was found to be approximately  $1.5 \phi_0/\mu s$  under de-

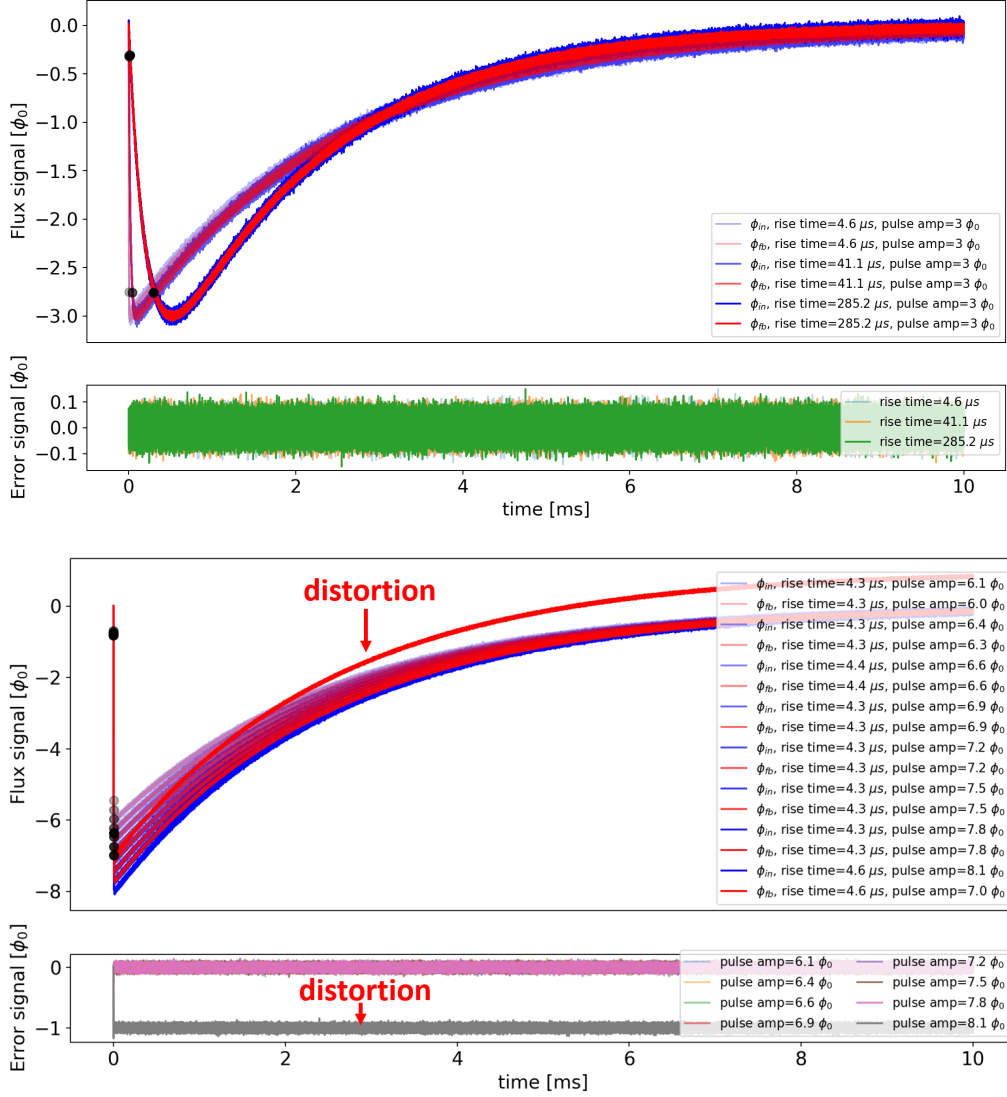


Fig. 11. Simulation of X-ray pulses with 22  $\mu$ A RMS noise. (a) Signal (blue lines) can be tracked well (red lines) when the rise time is not less than 4.3  $\mu$ s and the amplitude of pulse is 3  $\phi_0$ . (b) When the amplitude is larger than 7.8  $\phi_0$  and the rise time is about 4.3  $\mu$ s, signal distortion appears.

fault parameters in our model. The tracking capability of the system was validated with simulated X-ray pulse signals with different rise time (4.4 to 281  $\mu$ s) and amplitudes (6 to 8  $\phi_0$ ).

We hope that these simulation results will serve as a reference for the design of high-performance digital PID flux feedback electronic and multiplexing readout systems.

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